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TO:	Examiner, Connie C. Yoha	PHONE #:	
	Group Art Unit: 2818		
FROM:	Andrew C. Graham	DATE:	February 24, 2003
	Reg. No. 36,531		
SUBJECT:	Action Taken: Response to Office Action dated January 24, 2003		
	Application/Serial No.: 09/990,894		
	"INTEGRATED CIRCUIT MEMORY ARRAY WITH FAST TEST MODE UTILIZING MULTIPLE WORD LINE SELECTION AND METHOD THEREFOR"		
YOUR REF:		OUR REF:	023-0013
FACSIMILE #:	703-872-9318	PAGES:	4 (including this transmittal)
	(TC 2800 BF)		

MESSAGE**FAX RECEIVED****FEB 24 2003****TECHNOLOGY CENTER 2800**

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Roy E. Scheuerlein

Title: INTEGRATED CIRCUIT MEMORY ARRAY WITH FAST TEST MODE
UTILIZING MULTIPLE WORD LINE SELECTION AND METHOD
THEREFOR

Application No.: 09/990,894

Filed: November 16, 2001

Examiner: Connie C. Yoha

Group Art Unit: 2818

Atty. Docket No.: 023-0013

Box Non-Fee Amendment
COMMISSIONER FOR PATENTS
Washington, DC 20231**RESPONSE TO RESTRICTION REQUIREMENT**

This paper is responsive to an Office action dated January 24, 2003, having a shortened statutory period for response set to expire February 24, 2003.

Election of Invention

In response to the Examiner's Restriction Requirement, the undersigned provisionally elects Group I, being claims 1-39 and 50-54, with traverse.

AmendmentIn the Claims:

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FEB 24 2003

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40. (Amended) The integrated circuit defined by claim 29 wherein:
each memory cell comprises a passive element memory cell including an anti-fuse;
the X-line circuit comprises a first X-line circuit;
the first mode of operation comprises a read mode of operation;
the second mode of operation comprises a test mode of operation;
the first read circuit is for determining, in both the read and test modes of operation,
whether an aggregate read current of the one or more selected memory cells